# CLAIMS

1. A method for increasing the processing capability of a device, comprising:

requesting access to a module in a display controller;

processing continuously until notification by the module in the display controller, wherein a multiplexer in the display controller sends a first signal to a pin when the module is available; and

accessing the module in the display controller after receiving the first signal via the pin.

2. A method for increasing the processing capability of a device of claim 1, wherein requesting access to a module in a display controller includes transmitting a second signal to the module in the display controller.

3. A method for increasing the processing capability of a device of claim 1, wherein processing continuously until notification by the module in the display controller includes checking the pin in response to the first signal.

4. A method for increasing the processing capability of a device of claim 1, wherein processing continuously until notification by the module in the display controller includes selecting a wait signal or a busy signal from the multiplexer to transmit the first signal.

5. A method for increasing the processing capability of a device of claim 4, wherein selecting one of the wait signal and the busy signal from the multiplexer includes halting processing.

6. A method for increasing the processing capability of a device of claim 1, wherein requesting access to a module in a display controller further includes providing indirect addressing for communication.

7. A method, comprising:

transmitting a first signal from a first processor to a second processor;

routing the first signal to a module in the second processor, wherein the first signal indicates to the module that the first processor requires one of read and write access to the module;

selecting a second signal from one of a wait signal and a busy signal in a multiplexer on the second processor; and

processing continuously in the first processor until the receipt of the busy signal via a pin.

8. A method of claim 7, wherein selecting the second signal from one of the wait signal and the busy signal in the multiplexer on the second processor includes transmitting the busy signal to indicate to the first processor that the module is available for one of read and write access.

9. A method of claim 7, wherein processing continuously in the first processor until the receipt of the busy signal via the pin includes halting processing on the first processor.

10. A method of claim 7, wherein processing continuously in the first processor until the receipt of the busy signal via the pin includes receiving the signal.

11. A device, comprising:

a first processor coupled to a pin, the first processor being capable of continuously processing after transmitting a signal requesting access to a module in a second processor; and

a multiplexer in the second processor coupled to the pin, the pin being capable of notifying the first processor of the availability of the module in the second processor by the selection of one of a wait signal and a busy signal in the multiplexer.

12. A device of claim 11, wherein the second processor includes a combinatorial multiplexer coupled to the multiplexer, the combinatorial multiplexer being capable of routing signals from the module to the multiplexer.

13. A device of claim 12, wherein the module connects to the combinatorial multiplexer and an external module, the external module being external to the second processor.

14. A device of claim 11, wherein the pin is coupled to a plurality of registers in the second processor, the plurality of registers being capable of providing indirect addressing to the first processor.

15. A device of claim 11, wherein a signal propagates via a connection to the pin indicating the availability of the module, the signal being capable of halting processing on the first processor.

16. A device of claim 11, wherein the module is selected from the group consisting of a BitBLT module, a JPEG module, and an MPEG module.

17. A device of claim 11, wherein the first processor and the second processor communicate via indirect addressing.

18. A display controller configured to receive a first signal, comprising:

a plurality of first modules internal to the controller, the plurality of first modules being capable of accessing a plurality of second modules external to the controller;

a multiplexer coupled to the plurality of first modules via a combinatorial multiplexer, the multiplexer being capable of transmitting a second signal to a pin by selecting one of a wait signal and a busy signal in the multiplexer in response to the first signal; and

a connector coupled to the multiplexer and the pin, the connector being capable of transmitting the second signal to a source of the first signal.

19. A display controller configured to receive a first signal of claim 18, wherein the busy signal propagates via the connector.

20. A display controller configured to receive a first signal of claim 18, wherein the first signal is a transmission requesting one of read and write access to the plurality of first modules.

21. A display controller configured to receive a first signal of claim 18, wherein the second signal is a transmission from the plurality of first modules to the pin indicating the availability of the plurality of first modules for one of read and write access.

22. A display controller configured to receive a first signal of claim 18, wherein a first selector is capable of selecting one of a wait signal and a busy signal in the multiplexer.

23. A display controller configured to receive a first signal of claim 18, wherein a second selector in the combinatorial multiplexer is capable of selecting a module from the plurality of first modules.

24. A display controller configured to receive a first signal of claim 18, wherein the source of the first signal is a processor continuously processing.

25. A display controller configured to receive a first signal of claim 18, wherein the source communicates via indirect addressing.